AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method comprising:

receiving an echo signal at a transceiver, wherein the transceiver includes an Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC); and

reducing the echo signal with an echo rejecter at an input of the ADC, wherein the echo rejecter has an analog portion and a digital portion,

wherein the transceiver includes an analog front end (AFE), comprising:

a hybrid input stage;

a prebalance circuit;

the echo rejecter;

hybrid inputs;

receiver inputs;

transmitter outputs;

a high-pass filter circuit; and

a low-pass filter circuit.

2. (Previously Presented) The method of claim 1, further comprising:

minimizing any loss of ADC resolution with a data signal associated with the echo signal.

3. (Original) The method of claim 1, wherein the echo signal includes a transmitter noise signal.

4. (Canceled)

5. (Currently Amended) The method of claim [[4]] 1, wherein the AFE implements echo rejection across an entire usable frequency band.

6. (Previously Presented) The method of claim 3, further comprising:

lowering the transmitter noise signal and removing the echo signal completely with the digital portion of the echo rejecter.

7. (Currently Amended) The method of claim 6, further comprising:

designing ~~the~~ a high-pass filter circuit with a transmission line model; and

designing ~~the~~ a low-pass filter circuit with the transmission line model.

8. (Previously Presented) The method of claim 6, further comprising:

using the transceiver in a multiline communications system, wherein the multiline communications system treats multiple twisted copper pairs as a single multiline communications channel.

9. (Currently Amended) A system comprising:

means for receiving an echo signal at a transceiver, wherein the transceiver includes an Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC); and

means for reducing the echo signal with an echo rejecter at an input of the ADC, wherein the echo rejecter has an analog portion and a digital portion,

wherein the transceiver includes an analog front end (AFE), comprising:

a hybrid input stage;

a prebalance circuit;

the echo rejecter;

hybrid inputs;

receiver inputs;

transmitter outputs;

a high-pass filter circuit; and

a low-pass filter circuit.

10. (Previously Presented) The system of claim 9, further comprising:

means for minimizing any loss of ADC resolution with a data signal associated with the echo signal.

11. (Original) The system of claim 9, wherein the echo signal includes a transmitter noise signal.

12. (Canceled)

13. (Currently Amended) The system of claim [[12]] 9, wherein the AFE implements echo rejection across an entire usable frequency band.

14. (Previously Presented) The system of claim 11, further comprising:

means for lowering the transmitter noise signal and removing the echo signal completely with the digital portion of the echo rejecter.

15. (Currently Amended) The system of claim 14, further comprising:

means for designing ~~the~~ a high-pass filter circuit with a transmission line model; and

means for designing ~~the~~ a low-pass filter circuit with the transmission line model.

16. (Previously Presented) The system of claim 14, further comprising:

means for using the transceiver in a multiline communications system, wherein the multiline communications system treats multiple twisted copper pairs as a single multiline communications channel.

17-39. (Canceled)